

Improving SSD Performance Using Restricted Copyback Operations



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Impact and Major Factor of Data Copy 1

Data Copy Operation in SSD

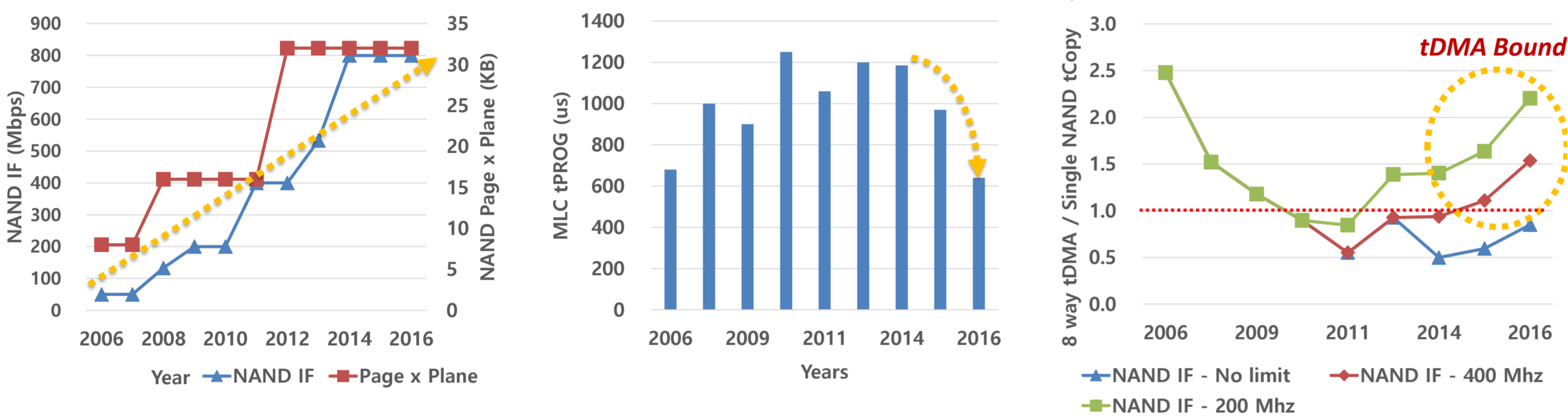
- Moving a large amount of data internally → Interfere host I/O
- E.g. Garbage Collection, Wear-leveling, Read Refresh

Data Copy Time, t_{Copy} (One Page per plane)

- On single NAND : $t_{Copy} = t_R + t_{DMA_{out}} + t_{DMA_{in}} + t_{PROG}$
- Multi way configuration : $t_{Copy} = t_R + (t_{DMA_{out}} + t_{DMA_{in}}) \times way + t_{PROG}$

Device Parameter Trend and relation with t_{Copy}

- NAND IF Speed (ONFI Spec.) ↑ : Decreasing t_{DMA}
 - NAND Page Size ↑ : Increasing t_{DMA}
 - NAND t_{PROG} ↓ : Decreasing t_{PROG}
 - Device Configuration (ch/way) : Multi ch / way
- Compensating each other
- t_{DMA} dominates the t_{Copy}**

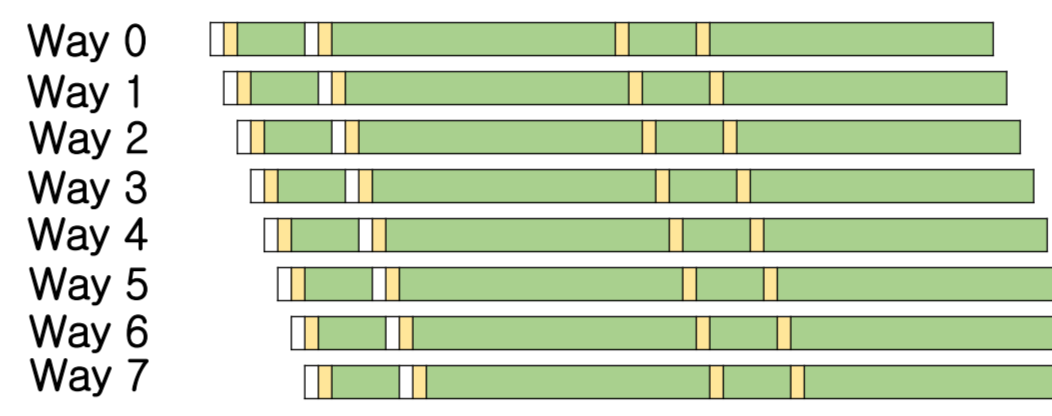


Copyback Operation in SSD 2

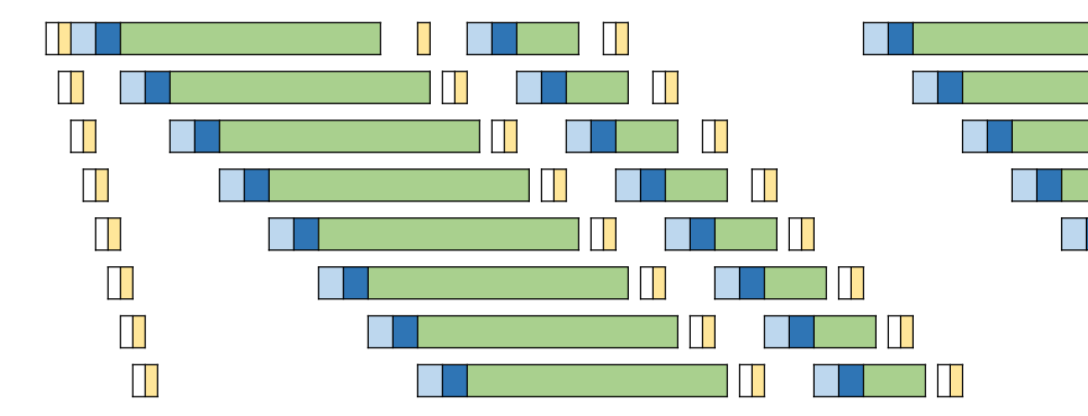
Advantage of copyback

- DMA time during data copy can be hidden
- $t_{DMA_{out}}$ and $t_{DMA_{in}}$ are not needed
- More effective when the number of channel/way is bigger

Data copy with Copyback



Data copy w/o Copyback



Difficulty of applying copyback in SSD

- Error Propagation Issue
- Consecutive copyback can cause **Uncorrectable Error**
- Same Plane Constraint
- Src/dst pages should be located in **Same Plane**
- Partial Invalid Page Management

Characterization of Copyback Error Propagation 3

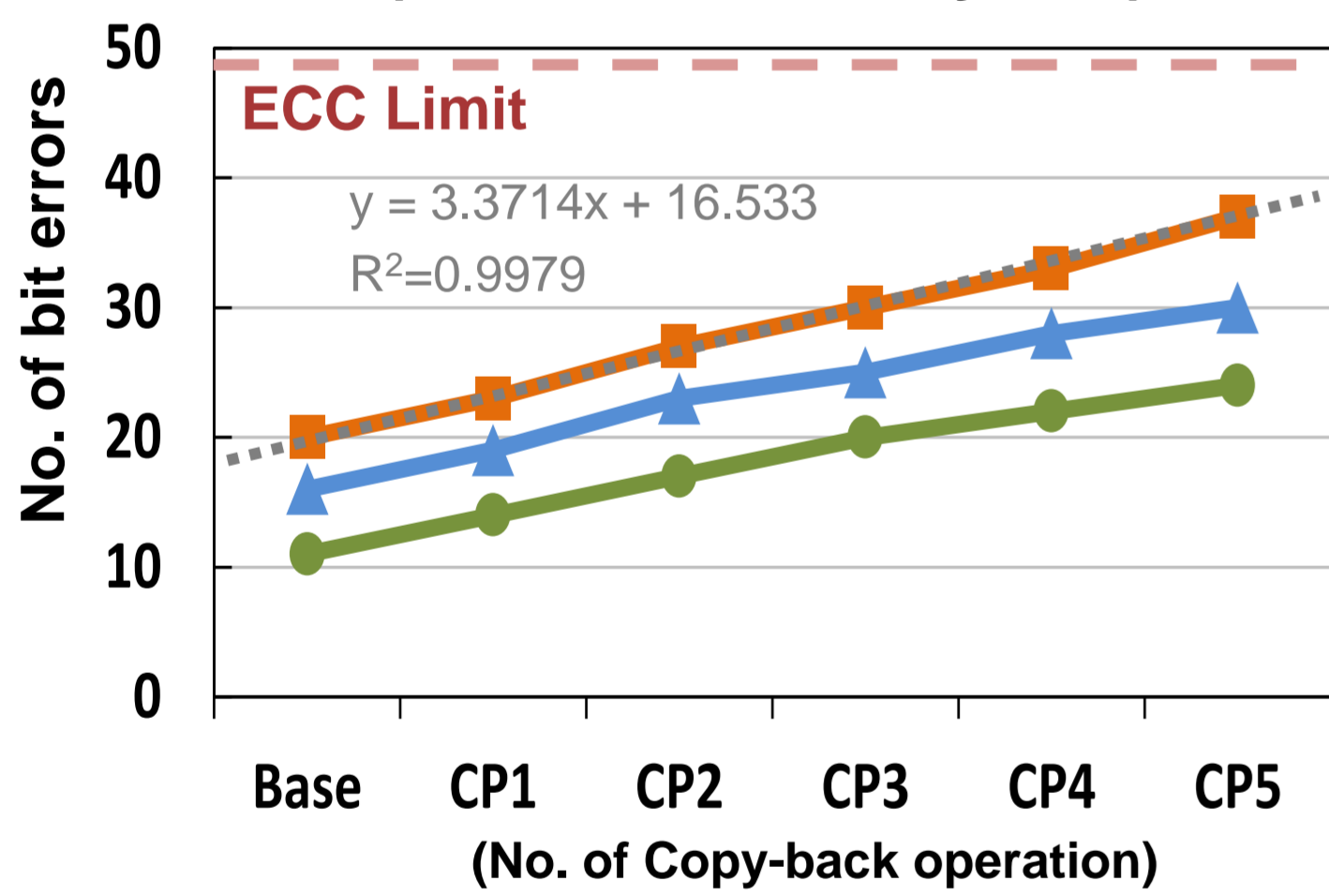
Bit Errors are increased by the number of Copyback

- 3~4 bits per each Copyback on 1x MLC NAND

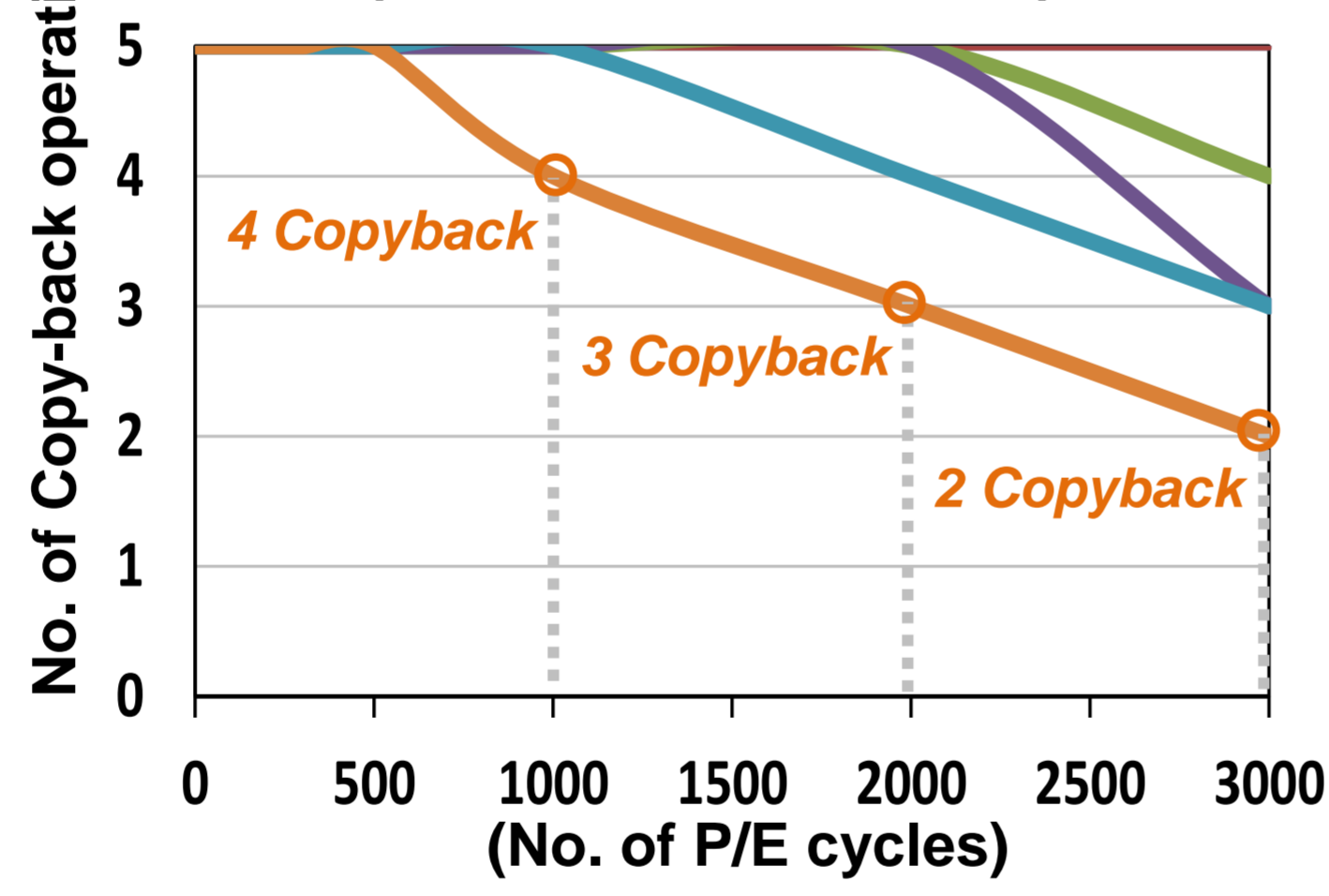
Minimum two Copyback is allowed at Max P/E cycle

- Without sacrificing retention (12 months)

Bit Errors vs. Copy-back Operation (After 3,000 P/E cycles)



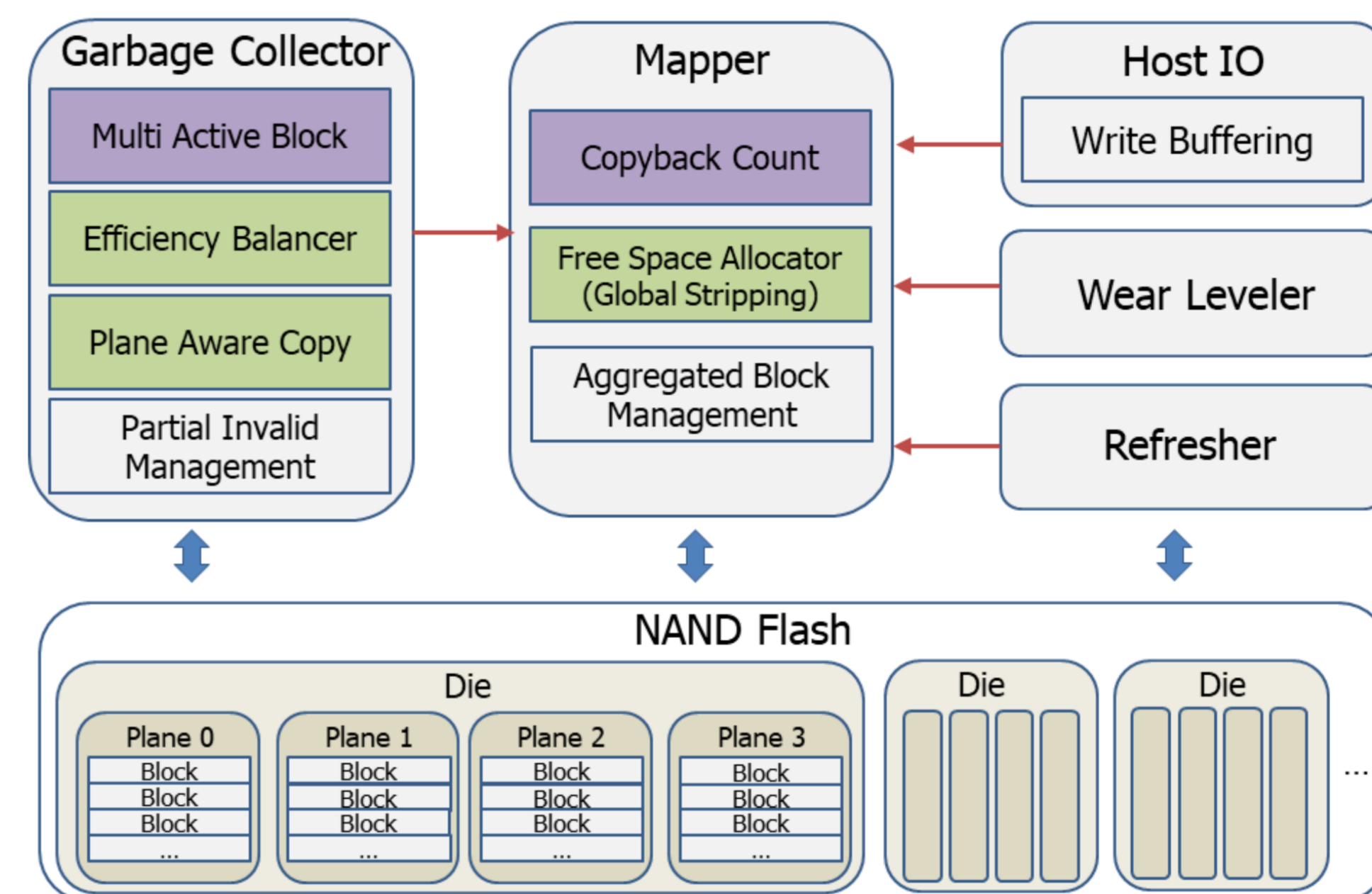
Allowable Copy-back Operation (After 30°C retention)



Legend for Bit Errors vs. Copy-back Operation:
 ● Min. Error WL (green)
 ▲ Avg. Error WL (blue)
 ■ Max. Error WL (orange)

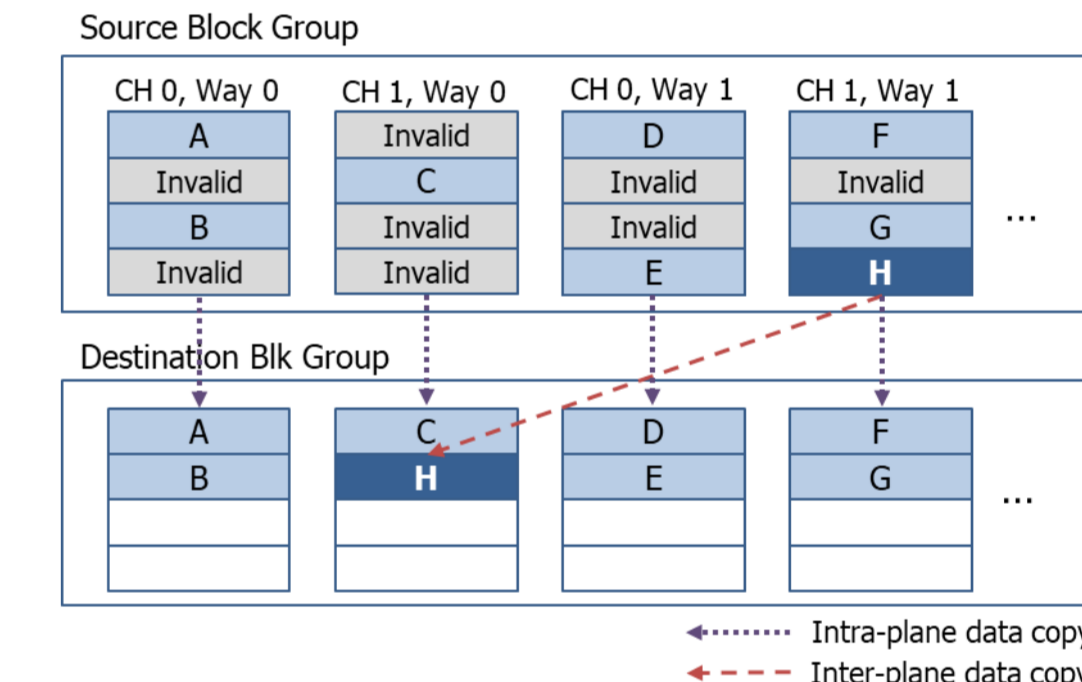
Legend for Allowable Copy-back Operation:
 — 0 month (blue)
 — 1 month (orange)
 — 2 month (green)
 — 3 month (purple)
 — 6 month (teal)
 — 12 month (red)

rcFTL : Restricted Copyback Aware FTL 4

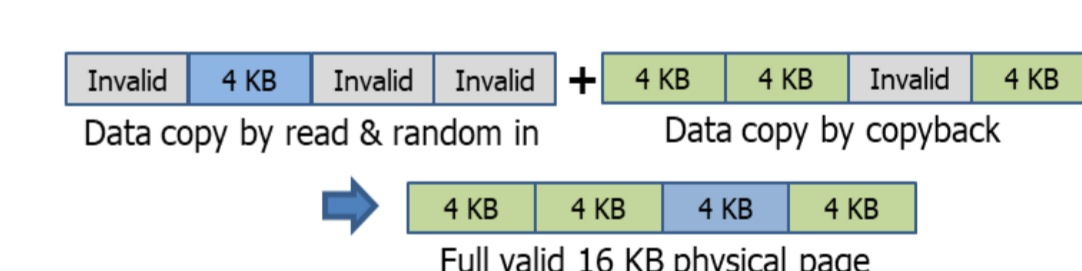


Plane Aware Copy

→ maximizing copyback usage



Partial Invalid Management (Physical Page > Mapping Size)



G.C Efficiency Balancer

- Preventing G.C efficiency difference between planes by managing victim block as a group

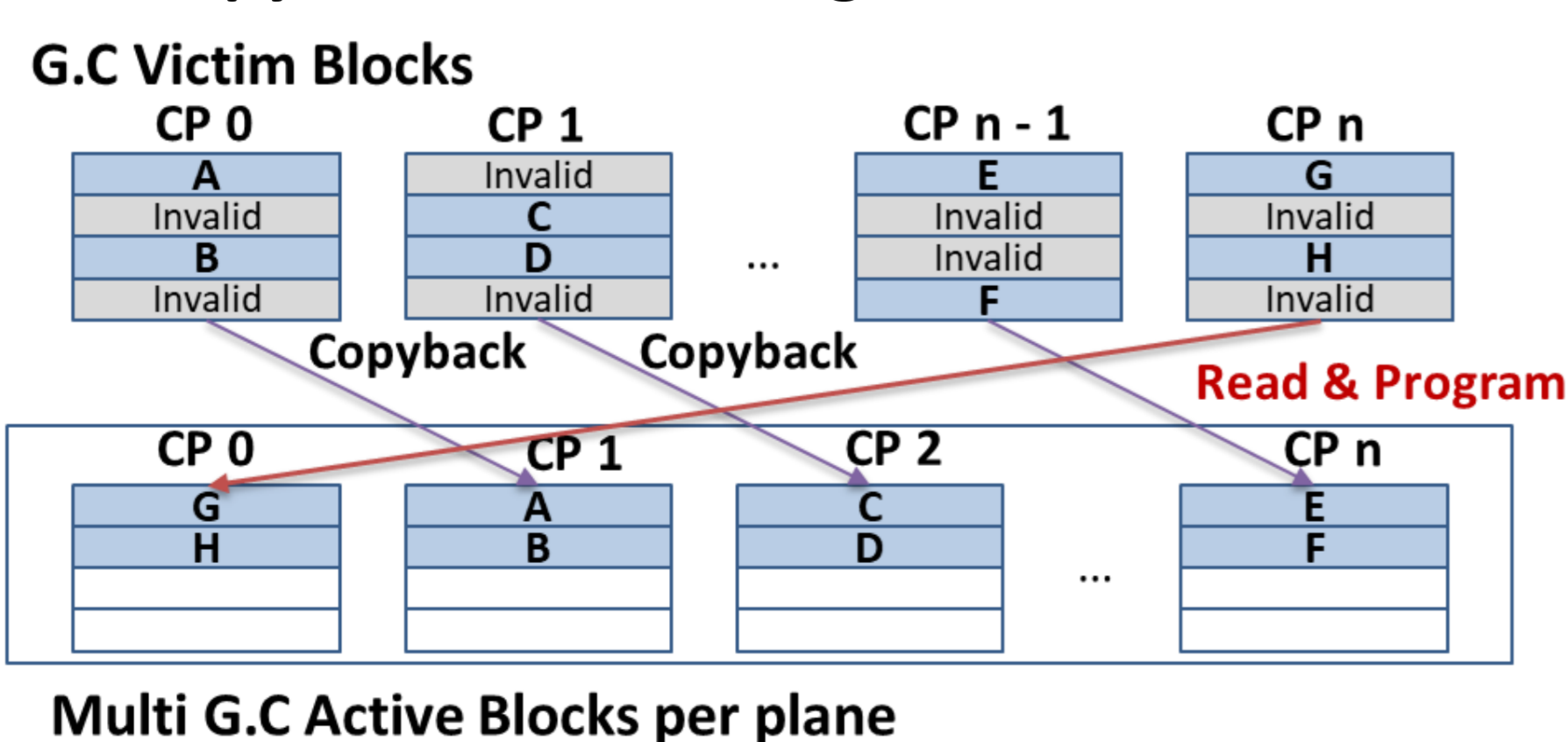
Plane Aware Copy / Partial Invalid Management

- Utilizing copyback maximally, minimizing inter plane data copy.

Design Requirements of rcFTL 5

Error Propagation Management

- R_Copyback : restricted version of copyback, executing error correction using off-chip ECC after n consecutive copyback
- Block based copyback count management to minimize overhead

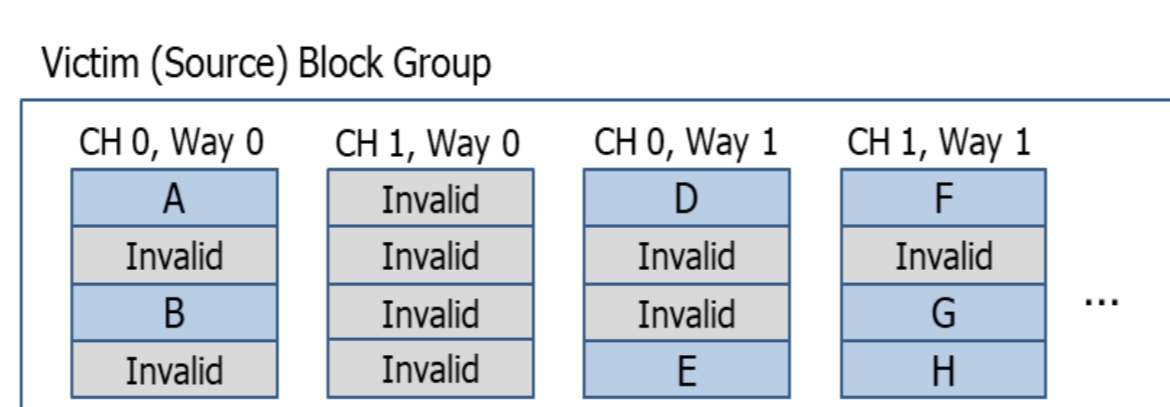


Same Plane Constraint

- Global Mapping Scheme
- Host workload independency, but GC efficiency difference per plane

GC Efficiency Balancing

- Doesn't allocate new victim block for specific plane until all blocks of victim group are invalidated
- valid page difference management (balancing)



Experimental Results 6

Performance improvement: up to 77.6%

- 8ch x 8way with Copyback up to 4 times (77.6%), 2 times (54.7%)
- Improvement of 8ch is higher than 4ch
- Improvement of 8way is higher than 2/4 way

