Computer Architecture **Spring 2014**

4190.308 **CSE (Jihong Kim)**

Course Information

March 3, 2014

■ Course Goal

This course introduces key components of modern digital computers, focusing on their functionalities and interactions. The course provides basic knowledge for building modern high-performance computer systems, emphasizing various design techniques.

■ Instructor and TAs

- Instructor: Jihong Kim 김지홍 (office: Room 328 @Building 302)

  Email: jihong@davinci.snu.ac.kr Phone: 880-8792

  Office hours: Tuesdays 17:00 ~ 18:00 a.m. (or by appointment)
- TAs: 박지성 (315-2@302, jspark@davinci.snu.ac.kr, 880-1861)

  김태진 (315-2@302, taejin1999@davinci.snu.ac.kr, 880-1861)

  Office hours: ToBeAnnounced (or by appointment)

  Lab Assistants: 전보영, 김도한, 전호윤, 김하종, 권혁준

■ Class Hours & Course Homepage

▷MW 15:30 ~ 16:45 @302-106

▷Course homepage: http://davinci.snu.ac.kr/courses/ca/2014_1/

- ▷ Important notices regarding the course will be announced in the course homepage. Please visit the course homepage regularly.
- ▷ Lecture slides will be available before the lecture at the homepage.

■ Prerequisite

▷Programming experience & logic design

■ **Textbook**

R. Bryant and D. O'Hallaron,

Computer Systems: A Programmer's Perspective, 2nd Edition, PEARSON.

■ **Grading**

▷ Midterm: 20% (mid-April)

▷ Final: 35% (mid-June)

▷ Assignments: 40%

▷ Attendance: 5%

▷ Course Repeat Policy: limited to A0 (i.e., no A+ for repeating students)

■ **Course Outline**

▷ We will cover the following topics:

- ▶ Instruction Set Architecture (ISA)
  - Instruction types
  - Addressing modes
  - RISC / CISC ISA styles
- ▶ Processor Architecture
  - Sequential architecture
  - Pipelined architecture
  - Advanced architectures
- ▶ Memory Hierarchy
  - Overall memory system organization
  - Principles of program locality
  - CPU cache memory
  - Virtual memory basics
- ▶ I/O Systems
  - I/O processing overview
  - Command registers / status registers / data registers
  - Interrupt mechanism
  - DMA
  - Sample I/O devices

■ **Assignments (Tentative)**

▷ 1 Assembly Programming Assignment

▷ 4~5 Processor Design Assignments

■ **Late Assignment Submission Policy**

▷ Each student has **3 bonus days** which can be used for any of the assignments.

(Note that you can use your bonus days only by *days*. For example, even if you are 2 hours late, you must use one full bonus day. No partial usage of a free late day is allowed.)

Once the 3 bonus days are exhausted, late submissions are accepted with large penalties:

1. If your assignment was *less than 24 hours*, the penalty is 10% of the TOTAL assignment points.
2. For each passing 24 hours, 20% penalty of the TOTAL assignment points is applied

■ **Cheating Policy**

For any type of cheating (e.g., copying others' assignments/programs, stealing an examination), if found, a grade of F will be assigned. For further disciplinary actions, the College of Engineering will be notified of the cheating activity.