Computer Architecture **Spring 2013**

4190.308 **CSE (Jihong Kim)**

Course Information

March 5, 2013

■ Course Goal

This course introduces key components of modern digital computers, focusing on their functionalities and interactions. The course provides basic knowledge for building modern high-performance computer systems, emphasizing various design techniques.

■ Instructor and TAs

- Instructor: Jihong Kim 김지홍 (office: Room 328 @Building 302)

  Email: jihong@davinci.snu.ac.kr Phone: 880-8792

  Office hours: Tuesdays 17:00 ~ 18:00 a.m. (or by appointment)

- TAs: Taejin Kim 김태진 (315-2@302, taejin1999@davinci.snu.ac.kr, 880-1861)

  Ji-Sung Park 박지성 (315-2@302, jspark@davinci.snu.ac.kr, 880-1861)

  Office hours: ToBeAnnounced (or by appointment)

  Lab Assistants: Bo-Yeong Jeon, Dohan Kim, Minwoo Kwak

■ Class Hours & Course Homepage

▷TTh 15:30 ~ 16:45 @302-107 (Lectured in English)

▷Course homepage: http://davinci.snu.ac.kr/courses/ca/2013_1/

- ▷ Important notices regarding the course will be announced in the course homepage. Please visit the course homepage regularly.
- ▷ Lecture slides will be available before the lecture at the homepage.

■ Prerequisite

▷Programming experience & logic design

■ **Textbook**

D. Patterson and J. Hennessy, *Computer Organization & Design, 4th Edition, Morgan-Kaufmann Publishers Inc., San Francisco, CA.*

■ **Useful Books for Assignments (These books are available for free from the homepage.)**

1. Arvind, R. S. Nikhil, J. Emer, and M Vijayaraghavan, *Computer Architecture: A Constructive Approach (Pre-Publication Draft)*, 2013.
2. R. S. Nikhil and K. Czeck, *BSV by Example*.

■ **Grading**

▷ Midterm: 20% (mid-April)

▷ Final: 35% (mid-June)

▷ Assignments: 40%

▷ Attendance: 5%

▷ Course Repeat Policy: limited to A0 (i.e., no A+ for repeating students)

■ **Course Outline (Tentative)**

▷ We will cover the following chapters from the textbook:

1. Introduction, Motivation, Computer Abstraction & Technology (Chapter 1)
2. Instruction Set Architecture (Chapter2 & Appendix B)
3. Performance Measurements & Evaluation (Chapter 1)
4. Simple Processor Implementation (Chapter 4)
5. Pipelined Processor Implementation (Chapter 4)
6. Memory Hierarchy (Chapter 5)
7. I/O Systems (Chapter 6)
8. Multiprocessor Overview (Chapter 7)

■ **Assignments (Tentative)**

▷ SMIPS Processor Design Labs Using BSV (Bluespec System Verilog)

- About 7 Design Assignments

■ **Assignment Submission Policy**

▷ All the assignments SHOULD be turned in before the due date.

Late submissions are accepted *for the following two cases only* with large penalties:

▷ If your assignment was late *by less than 24 hours*, the penalty is 10% of the TOTAL assignment points.

▷ For each passing 24 hours, the 10% penalty of the TOTAL assignment points is applied

■ **Cheating Policy**

For any type of cheating (e.g., copying others' assignments/programs, stealing an examination), if found, a grade of F will be assigned. For further disciplinary actions, the College of Engineering will be notified of the cheating activity.